REMARKS

Claims 10-17 are pending in the present application. The Office Action and cited references have been considered. Favorable reconsideration is respectfully requested.

Claims 10-17 were rejected under 35 U.S.C. §102 (b) as being anticipated by Larner et al. (US 6,104,638). This rejection is respectfully traversed for the following reasons.

Claim 10 now recites a method for restoring administrative data records of a nonvolatile memory that can be written in units of sectors and erased in units of blocks, the records being stored in a more rapidly accessible internal volatile flag memory of an assigned memory controller. The method includes, setting up, in one or more memory blocks of the nonvolatile memory, a contiguous reconstruction table for administrative memory data (RKT), and continually updating the reconstruction table with records of all write and erase operations in the nonvolatile memory out of the internal flag memory. The step of continually updating comprises recording all information with which the administrative data records of the internal flag memory of the memory controller can be completely reconstructed in each case during a restart after a power failure. The method further includes starting a reconstruction when a predefined fill level of the reconstruction table (RKT) is reached, in each case to create a defined initial state of the administrative data records in the flag memory and in the reconstruction table (RKT), and recording the start of the reconstruction as a last entry (OE) in the reconstruction table. This is not taught, disclosed or made obvious by the prior art of record.

The remarks submitted in the amendment filed on April 26, 2007, incorporated by reference herein. In addition, Applicant submits the following arguments.

Larner describes a processor system with a RAM and a non-volatile memory, which is arranged in individually erasable segments, also called blocks. The patent relates to a method to synchronize the values of administrative data words (parameters) in the RAM with previously updated data words which were continuously written to at least two reserved segments of the non-volatile memory. At the beginning of a segment, a special ID with a counter value is written, and the end of the relevant data entries is found by an entry, which has the value of an erased memory location. The synchronizing is done by reading all relevant entries and overwriting the corresponding memory location in the RAM until an empty entry is found. As the first segment is filled up, the second segment is filled with current data words from RAM and the first segment is erased. The next updating is done in the second segment until this is filled up again. Then the segments are swapped again.

Applicant's application also relates to a method to update memory locations in RAM from a reconstruction table in the non-volatile memory. The difference between the claimed invention and Larner lies in the method for the reconstruction of the table and which types of entries for which the method is utilized. According to Applicant's invention, the reconstruction table has a fixed length and is optimized for memory administration data. There are tables holding the relation between logical and physical addresses and the addresses of alternate sectors, to which data is written until a sector is filled. These tables of memory administration data can be brought into a defined state that corresponds to the state used at the initial start of the memory system. When the entries fill up the reconstruction table, a reorganization is started which brings the memory administration data into the defined state. This start is marked with a special start-entry (OE). The end of the reorganization process is also

marked with a special end-entry (FE). If the end-entry (FE) is encountered, all entries before that are no longer relevant.

To emphasize that the method is related to the reconstruction of memory administration data, claim 10 has been amended to recite "a contiguous reconstruction table for memory administration data." Support for this amendment can be found on, e.g., on page 3, lines 1-2. The method of Larner is not optimized for memory administration data and does not teach or suggest a reorganization process.

In Larner, there is no reorganization process to bring the administrative data into a defined initial state. Larner only describes a reconstruction process to synchronize the values in the RAM and in the reconstruction table to the same current values. The administrative data of Larner do not have a defined initial state. They tend to become larger and larger. The claimed invention anticipates initial states of the data, such as initial values in allocation tables for memory addresses. The reorganization process brings the data into defined initial states which correspond to a new memory. Such a reorganization is marked with special entries in the reconstruction table. This is different to the end-of-table (FFFFhex). Both methods have such an end-of-table value behind the last written entry. Larner does not use a reorganization and so there is no start-of reorganization marker (OE). There is also marker for the successful reorganization (FE). Both markers can not be found in the Patent of Larner.

The reorganization of the reconstruction table is not done by reading the actual values of the parameters from RAM. The reorganization is done by bringing the administrative memory data into an initial state and marking this process in the reconstruction table with the different entries FE and OE. This reorganization is not anticipated by Larner, as there is only an

end-of-table-marker (FFFFhex) and a counter at the beginning of the table, which is not sufficient for the reorganization process.

In claim 10 it is stated that the administrative memory data is brought into an initial state. It is clear that the reconstruction tables are in an initial state after a reorganization, which is the erased state.

As stated above, the end-of-table-marker FFFF is not sufficient to control the reorganization process as claimed in this application.

In view of these differences, Applicant respectfully submits that Larner does not disclose Applicant's claimed invention arranged as in claim 10. Applicant further submits that claims 11-17 are patentable at least for the reasons discussed above with respect to claim 10. Specifically, with respect to claim 13, Applicant respectfully submits that thefeature of claim 13 is different than the counter of Larner because it uses the marker for successful reorganization (FE), which is not found in Larner.

In the view of the above amendment and remarks, Applicant respectfully submits that claims 10-17 are patentable over the prior art of record. Applicant requests reconsideration and withdrawal of the outstanding rejections of record. Applicant submits that the application is now in condition for allowance and early notice to this effect is most earnestly solicited.

If the Examiner has any questions, he is invited to contact the undersigned at 202-628-5197.

Respectfully submitted,

BROWDY AND NEIMARK, P.L.L.C.
Attorneys for Applicant(s)

By /Ronni S. Jillions/
Ronni S. Jillions
Registration No. 31,979

RSJ:srd
Telephone No.: (202) 628-5197
Facsimile No.: (202) 737-3528
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